

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI Scheme of Teaching and Examination: 2018-19 M.Tech in VLSI Design & Embedded Systems (EVE) Choice Based Credit System (CBCS)											
I SEMESTER											
Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits	
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks		
1	PCC	18ELD11	Advanced Engineering Mathematics	04	--	03	40	60	100	4	
2	PCC	18EVE12	ASIC Design	04	--	03	40	60	100	4	
3	PCC	18EVE13	Advanced Embedded System	04	--	03	40	60	100	4	
4	PCC	18EVE14	VLSI Testing	04	--	03	40	60	100	4	
5	PCC	18EVE15	Digital VLSI Design	04	--	03	40	60	100	4	
6	PCC	18EVEL16	VLSI & ES Lab-1	-	04	03	40	60	100	2	
7	PCC	18RMI17	Research Methodology and IPR	02	--	03	40	60	100	2	
TOTAL				22	04	21	280	420	700	24	
Note:- PCC: Professional Core Course											
Internship: All the students shall undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. University examination will be conducted during III semester and prescribed credit shall be included in the III semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as failed and have to complete during subsequent University examination after satisfying the internship requirements.											

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI										
Scheme of Teaching and Examination: 2018-19										
M.Tech in VLSI Design & Embedded Systems (EVE)										
Choice Based Credit System (CBCS)										
II SEMESTER										
Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18EVE21	Design of Analog and Mixed mode VLSI Circuits	04	--	03	40	60	100	4
2	PCC	18EVE22	Real Time Operating System	04	--	03	40	60	100	4
3	PCC	18EVE23	System Verilog	04	--	03	40	60	100	4
4	PEC	18XXX24X	Professional Elective 1	04	--	03	40	60	100	4
5	PEC	18XXX25X	Professional Elective 2	04	--	03	40	60	100	4
6	PCC	18EVEL26	VLSI & ES Lab-2	--	04	03	40	60	100	2
7	PCC	18EVE27	Technical Seminar	--	02	--	100	--	100	2
TOTAL				20	06	18	340	360	700	24
Note:- PCC: Professional Core Course, PEC: Professional Elective Course										
Professional Elective 1				Professional Elective 2						
Course Code Under 18XXX24X		Course Title		Course Code Under 18XXX25X		Course Title				
18EVE241		Advances in VLSI Design		18EVE251		Low Power VLSI Design				
18EVE242		Nanoelectronics		18EVE252		SoC Design				
18EVE243		Static Timing Analysis		18ELD253		Micro Electro Mechanical Systems				
Note:										
1. Technical Seminar: CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide in any and a senior faculty of the department. Participation in seminar by all postgraduate students of the same and other semesters of the programme shall be mandatory. The CIE marks awarded for Technical Seminar, shall be based on the evaluation of Seminar Report, Presentation skill and Question and Answer session in the ratio 50:25:25.										
2. Internship: All the students shall undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. A University examination will be conducted during III semester and prescribed credit shall be included in the III semester. Internship shall be considered as head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as failed and have to complete during subsequent University examination after satisfying the internship requirements.										

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI										
Scheme of Teaching and Examination: 2018-19										
M.Tech in VLSI Design & Embedded Systems (EVE)										
Choice Based Credit System (CBCS)										
III SEMESTER										
Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination			Credits	
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks		Total Marks
1	PCC	18EVE31	CAD of Digital Systems	04	--	03	40	60	100	4
2	PEC	18XXX32X	Professional Elective 3	04	--	03	40	60	100	4
3	PEC	18XXX33X	Professional Elective 4	04	--	03	40	60	100	4
4	Proj	18EVE34	Evaluation of Project Phase -1	--	02	--	100	--	100	2
5	INT	18EVE35	Internship	(Completed during the intervening vacation of I and II semesters and /or II and III semesters.)		03	40	60	100	6
TOTAL				12	02	12	260	240	500	20
Note:- PCC: Professional Core Course, PEC: Professional Elective Course, Proj: Project, INT: Internship										
Professional Elective 3					Professional Elective 4					
Course Code Under 18XXX32X	Course Title			Course Code Under 18XXX33X	Course Title					
18ECS321	Advances in Image Processing			18EVE331	VLSI for Signal Processing					
18EVE322	CMOS RF Circuit Design			18ESP332	Pattern Recognition & Machine Learning					
18EVE323	Embedded Linux System Design And Development			18ECS333	Internet of Things					
Note:										
<p>1. Project Phase-1: Students in consultation with the guide/co-guide if any, shall pursue literature survey and complete the preliminary requirements of selected Project work. Each student shall prepare relevant introductory project document, and present a seminar. CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide and a senior faculty of the department. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.</p> <p>SEE (University examination) shall be as per the University norms.</p> <p>2. Internship: Those, who have not pursued /completed the internship shall be declared as failed and have to complete during subsequent University examinations after satisfy the internship requirements.</p> <p>Internship SEE (University examination) shall be as per the University norms.</p>										

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI Scheme of Teaching and Examination: 2018-19 M.Tech in VLSI Design & Embedded Systems (EVE) Choice Based Credit System (CBCS)										
IV SEMESTER										
Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks Viva voce	Total Marks	
1	Proj	18EVE41	Project Work Phase -2	--	04	03	40	60	100	20
TOTAL				--	04	03	40	60	100	20
Note: Proj: Project.										
Note: 1. Project Phase-2: CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any and a Senior faculty of the department. The CIE marks awarded for Project Work Phase -2, shall be based on the evaluation of Project Report subjected to plagiarism check, Project Presentation skill and Question and Answer session in the ratio 50:25:25. SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check, shall be as per the University norms.										