K. S. SCHOOL OF ENGINEERING AND MANAGEMENT

Department of Electronics and Communication Engineering

Electronic Devices and Instrumentation Laboratory

LIST OF EXPERIMENTS

PART A: Experiments using discrete components

- Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative).
- Half wave rectifier and Full wave rectifier with and without filter and measure the ripple factor.
- Characteristics of Zener diode and design a Simple Zener voltage regulator determine line and load regulation.
- Characteristics of LDR and Photo diode and turn on an LED using LDR
- Static characteristics of SCR.
- SCR Controlled HWR and FWR using RC triggering circuit
- Conduct an experiment to measure temperature in terms of current/voltage using a temperature sensor bridge.
- Measurement of Resistance using Wheatstone and Kelvin's bridge.

PART-B: Simulation using EDA Software

(EDWinXP, PSpice, MultiSim, Proteus, Circuit Lab or any equivalent tool)

- Input and Output characteristics of BJT Common emitter configuration and evaluation of parameters.
- Transfer and drain characteristics of a JFET and MOSFET.
- UJT triggering circuit for Controlled Full wave Rectifier.
- Design and simulation of Regulated power supply.

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Digital System Design Laboratory

LIST OF EXPERIMENTS

- Verify

  (i) DeMorgan's Theorem for 2 variables.

  (ii) The sum-of product and product-of-sum expressions using universal gates.

- Design and implement

  (i) Half Adder & Full Adder using i) basic gates. ii) NAND gates

  (ii) Half subtractor& Full subtractor using i) basic gates ii) NAND gates

- Design and implement

  (i) 4-bitParallelAdder/Subtractor using IC 7483.

  (ii) BCD to Excess-3 code conversion and vice-versa.

- Design and Implementation of

  (i) 1-bit Comparator

  (ii) 5-bit Magnitude Comparator using IC 7485.

- Realize

  (i) Adder & Subtractors using IC 74153.

  (ii) 4-variable function using IC74151 (8:1MUX).

- Realize

  (i) Adder & Subtractors using IC74139.

  (ii) Binary to Gray code conversion & vice-versa (74139)

- Realize the following flip-flops using NAND Gates. Master-Slave JK, D & T Flip-Flop.
- Realize the following shift registers usingIC7474/7495

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(i) SISO (ii) SIPO (iii)) PISO(iv))PIPO (v) Ring (vi) Johnson counter

- Realize

  (i) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop

  (ii) Mod-N Counter using IC7490 / 7476

  (iii) Synchronous counter using IC74192

- Design Pseudo Random Sequence generator using 7495. L2, L3
- Design Serial Adder with Accumulator and simulate using Simulation tool.
- Design Binary Multiplier and simulate using Simulation tool..

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Digital Signal Processing Laboratory

LIST OF EXPERIMENTS

- Verification of sampling theorem.
- Linear and circular convolution of two given sequences, Commutative, distributive and associative property of convolution.
- Auto and cross correlation of two sequences and verification of their properties
- Solving a given difference equation.
- Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum (using DFT equation and verify it by built-in routine).
- (i) Verification of DFT properties (like Linearity and Parsevals theorem, etc.)
- (ii) DFT computation of square pulse and Sinc function etc.
- Design and implementation of FIR filter to meet given specifications (using different window techniques).
- Design and implementation of IIR filter to meet given specifications
- Linear convolution of two sequences
- Circular convolution of two sequences
- N-point DFT of a given sequence
- Impulse response of first order and second order system.
- Implementation of FIR filters.

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Hardware Description Language Laboratory

LIST OF EXPERIMENTS

Part–A: PROGRAMMING

- Write Verilog code to realize all the logic gates
- Write a Verilog program for the following combinational designs

  a. 2 to 4 decoder

  b. 8 to 3 (encoder without priority & with priority)

  c. 8 to 1 multiplexer.

  d. 4 bit binary to gray converter

  e. Multiplexer, de-multiplexer, comparator.

- Write a VHDL and Verilog code to describe the functions of a Full Adder using three modeling styles.
- Write a Verilog code to model 32 bit ALU using the schematic diagram shown below

  ALU should use combinational logic to calculate an output based on the four bit op-code input.

  ALU should pass the result to the out bus when enable line in high, and tri-state the out bus when the enable line is low.

  ALU should decode the 4 bit op-code according to the example given below.

- Develop the Verilog code for the following flip-flops, SR, D, JK and T.
- Design a 4 bit binary, BCD counters (Synchronous reset and Asynchronous reset) and —any sequence counters, using Verilog code.

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Part–B:INTERFACING (at least four of the following must be covered using VHDL/Verilog)

- Write HDL code to display messages on an alpha numeric LCD display.
- Write HDL code to interface Hex key pad and display the key code on seven segment display.
- Write HDL code to control speed, direction of DC and Stepper mor.
- Write HDL code to accept Analog signal, Temperature sensor and display the data on LCD or Seven segment displays.
- Write HDL code to generate different waveforms (Sine, Square, Triangle, Ramp etc.,) using DAC - change the frequency.
- Write HDL code to simulate Elevator operation.

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Advanced Communication Laboratory

LIST OF EXPERIMENTS

PART-A: Following Experiments No. 1 to 4 has to be performed using discrete Components

- Time Division Multiplexing and Demultiplexing of two bandlimited signals.
- ASK generation and detection
- FSK generation and detection
- PSK generation and detection
- Measurement of frequency, guide wavelength, power, VSWR and attenuation in microwave test bench.
- Measurement of directivity and gain of microstrip dipole and Yagi antennas.
- Determination of

  a. Coupling and isolation characteristics of microstrip directional coupler.

  b. Resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.

  c. Power division and isolation of microstrip power divider.

- Measurement of propagation loss, bending loss and numerical aperture of an optical fiber.

PART-B: Simulation Experiments using SCILAB/MATLAB/Simulink or LabVIEW

- Simulate NRZ, RZ, half-sinusoid and raised cosine pulses and generate eye diagram for binary polar signaling.
- Simulate the Pulse code modulation and demodulation system and display the waveforms.

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- Simulate the QPSK transmitter and receiver. Plot the signals and its constellation diagram.
- Test the performance of a binary differential phase shift keying system by simulating the non-coherent detection of binary DPSK.

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VLSI Laboratory

LIST OF EXPERIMENTS

PART - A
ASIC-DIGITAL DESIGN

- Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library with given constraints*. Do the initial timing verification with gate level simulation.
    - An inverter
    - A Buffer
    - Transmission Gate
    - Basic/universal gates
    - Flip flop -RS, D, JK, MS, T
    - Serial & Parallel adder
    - 4-bit counter [Synchronous and Asynchronous counter]
    - Successive approximation register [SAR]

PART - B
ANALOG DESIGN

- Design an Inverter with given specifications**, completing the design flow mentioned below:
    - Draw the schematic and verify the following
        - DC Analysis
        - Transient Analysis
    - Draw the Layout and verify the DRC, ERC
    - Check for LVS
    - Extract RC and back annotate the same and verify the Design
    - Verify & Optimize for Time, Power and Area to the given constraint*
- Design the (i) Common source and Common Drain amplifier and (ii) A Single
- Stage differential amplifier, with given specifications**, completing the

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- design flow mentioned below:
    - Draw the schematic and verify the following
        - DC Analysis
        - AC Analysis
        - Transient Analysis
    - Draw the Layout and verify the DRC, ERC
    - Check for LVS
    - Extract RC and back annotate the same and verify the Design.
- Design an op-amp with given specification** using given differential amplifier
- Common source and Common Drain amplifier in library*** and completing the
- design flow mentioned below:
    - Draw the schematic and verify the following
        - DC Analysis
        - ii). AC Analysis
        - Transient Analysis
    - Draw the Layout and verify the DRC, ERC
    - Check for LVS
    - Extract RC and back annotate the same and verify the Design.
- Design a 4 bit R-2R based DAC for the given specification and completing the design flow mentioned using given op-amp in the library***.
    - Draw the schematic and verify the following
        - DC Analysis
        - AC Analysis
        - Transient Analysis
    - Draw the Layout and verify the DRC, ERC
- For the SAR based ADC mentioned in the figure below draw the mixed signal schematic and verify the functionality by completing ASIC Design FLOW. [Specifications to GDS-II]

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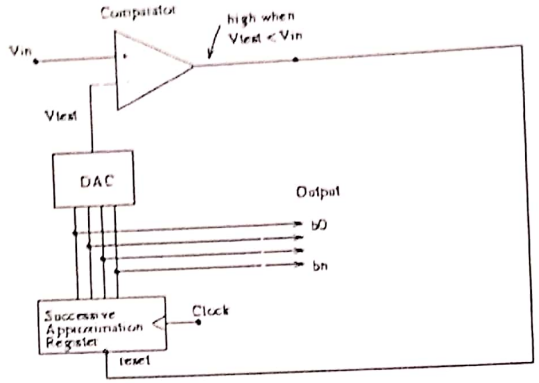

- An appropriate constraint should be given.
- ** Appropriate specification should be given.
- *** Applicable Library should be added & information should be given to the Designer

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